

United States Patent and Trademark Office

ml

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.usplo.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/840,169	05/06/2004	Myoung-Kwan Kim	51922/P849	7507
23363 7590 07/13/2007 CHRISTIE, PARKER & HALE, LLP		EXAMINER		
PO BOX 7068			SHAPIRO, LEONID	
PASADENA, CA 91109-7068			ART UNIT	PAPER NUMBER
			2629	
			MAIL DATE	DELIVERY MODE
		•	07/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	· · · · · · · · · · · · · · · · · · ·	Application No.	Applicant(s)		
Office Action Summary		10/840,169	KIM ET AL.		
		Examiner	Art Unit		
		Leonid Shapiro	2629		
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply					
A SH WHIC - Exte after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DANS IN ITEM 1.13 SIX (6) MONTHS from the mailing date of this communication. O period for reply is specified above, the maximum statutory period we tree to reply within the set or extended period for reply will, by statute, reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim rill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).		
Status			.*		
 Responsive to communication(s) filed on <u>06 May 2004</u>. This action is FINAL. 2b) ☐ This action is non-final. Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i>, 1935 C.D. 11, 453 O.G. 213. 					
Dispositi	ion of Claims				
4) Claim(s) 1-28 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) is/are allowed. 6) Claim(s) 1-5,13-17 and 24-26 is/are rejected. 7) Claim(s) 6-12,18-23,27 and 28 is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement.					
Application Papers					
10)	The specification is objected to by the Examiner The drawing(s) filed on is/are: a) access Applicant may not request that any objection to the Replacement drawing sheet(s) including the correction The oath or declaration is objected to by the Example 1.	epted or b) objected to by the Edrawing(s) be held in abeyance. See on is required if the drawing(s) is obj	e 37 CFR 1.85(a). ected to. See 37 CFR 1.121(d).		
Priority (ınder 35 U.S.C. § 119		•		
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 					
	t(s) se of References Cited (PTO-892) se of Draftsperson's Patent Drawing Review (PTO-948)	4)			
3) Infor	nation Disclosure Statement(s) (PTO/SB/08) No(s)/Mail Date	5) Notice of Informal P			

Art Unit: 2629

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 1. Claims 1-2,13-14,24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (6,191,762 B1) in view of Jeddeloh (6,157,398).

As to claims 1-2 Kim teaches an address data processor for a plasma display panel (PDP) (Col. 1, lines 6-10), comprising:

a subfield data generator for receiving RGB video data, and generating corresponding subfield data (fig. 1, item 14a, col. 1, lines 25-27 and 59-63);

a frame memory for storing the subfield data, and outputting the stored subfield data (fig. 1, item 14b, col. 1, lines 25-29); and

a subfield data arranger for receiving the subfield data output by the frame memory, arranging the subfield data as address data for each subfield, and outputting the address data to represent gray on the PDP (fig. 1, item 14c, from col. 1, line 59 to col. 2, line 8).

Kim does not disclose using a rising edge and a falling edge of a reference clock signal.

Jeddeloh teaches to enables the transfers to the frame memory on both a rising edge and a falling edge of a reference clock signal (fig.2, items 156,162, col. 4, lines 20-40).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Jeddeloh teachings into Kim system in order to enable pipelining (col. 4, lines 30-40 in the Jeddeloh reference).

As to claims 13-14, Kim teaches a method processing data for a plasma display panel (PDP) (Col. 1, lines 6-10), comprising:

- a) generating subfield data corresponding to RGB input video data (fig. 1, item 14a, col. 1, lines 25-27 and 59-63);
- b) storing the subfield data in a frame (fig. 1, item 14b, col. 1, lines 25-29); c) reading the subfield data stored in the frame memory (fig. 1, item 14b, col. 1, lines 25-29); and
- (d) arranging the subfield data read from the frame memory as address data for each subfield, and outputting the address data to the PDP to represent gray on the PDP (fig. 1, item 14c, from col. 1, line 59 to col. 2, line 8).

Kim does not disclose using a rising edge and a falling edge of a reference clock signal.

Jeddeloh teaches to enables the transfers to the frame memory on both a rising edge and a falling edge of a reference clock signal (fig.2, items 156,162, col. 4, lines 20-40).

Application/Control Number: 10/840,169

Art Unit: 2629

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Jeddeloh teachings into Kim system in order to enable pipelining (col. 4, lines 30-40 in the Jeddeloh reference).

As to claim 24, Kim teaches in a method processing data in a plasma display panel (PDP), a recording medium for storing a program for performing address data processing operations (Col. 1, lines 6-10), comprising:

- a) generating subfield data corresponding to RGB input video data (fig. 1, item 14a, col. 1, lines 25-27 and 59-63);
- b) storing the subfield data in a frame (fig. 1, item 14b, col. 1, lines 25-29); c) reading the subfield data stored in the frame memory (fig. 1, item 14b, col. 1, lines 25-29); and
 - (d) arranging the subfield data read from the frame memory as address data for each subfield, and outputting the address data to the PDP to represent gray on the PDP (fig. 1, item 14c, from col. 1, line 59 to col. 2, line 8).

Kim does not disclose using a rising edge and a falling edge of a reference clock signal.

Jeddeloh teaches to enables the transfers to the frame memory on both a rising edge and a falling edge of a reference clock signal (fig.2, items 156,162, col. 4, lines 20-40).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Jeddeloh teachings into Kim system in order to enable pipelining (col. 4, lines 30-40 in the Jeddeloh reference).

Page 5

As to claim 25-26 Kim teaches an address data processor for a plasma display panel (PDP) (Col. 1, lines 6-10), comprising:

a subfield data generator for receiving video data having at least color, and generating corresponding subfield data (fig. 1, item 14a, col. 1, lines 25-27 and 59-63);

a frame memory for storing the subfield data, and outputting the stored subfield data (fig. 1, item 14b, col. 1, lines 25-29); and

a subfield data arranger for receiving the subfield data output by the frame memory, arranging the subfield data as address data for each subfield, and outputting the address data to represent gray on the PDP (fig. 1, item 14c, from col. 1, line 59 to col. 2, line 8).

Kim does not disclose using a rising edge and a falling edge of a reference clock signal.

Jeddeloh teaches to enables the transfers to the frame memory on both a rising edge and a falling edge of a reference clock signal (fig.2, items 156,162, col. 4, lines 20-40).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Jeddeloh teachings into Kim system in order to enable pipelining (col. 4, lines 30-40 in the Jeddeloh reference).

2. Claims 3-4,15-16 are rejected under 35 U:S.C. 103(a) as being unpatentable over Kim and Jeddeloh as applied to claim 1 above, and further in view of Nagai (6,608,610 B2).

Application/Control Number: 10/840,169 Page 6

Art Unit: 2629

Kim and Jeddeloh do not disclose an RGB mixer for receiving the RGB video data, selecting data as a specific combination of the RGB video data, and outputting the selected data to the subfield data generator.

Nagai teaches an RGB mixer for receiving the RGB video data, selecting data as a specific combination of the RGB video data, and outputting the selected data to the subfield data generator (fig. 1A, items 14-15, col. 9, lines 36-47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Nagai teachings into Kim and Jeddeloh system in order to response to signal format (col. 1, lines 36-38 in the Nagai reference).

3. Claims 5,17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagai, Kim and Jeddeloh as applied to claim 4 above, and further in view of Sha et al (7,142,251 B2).

Nagai, Kim and Jeddeloh do not disclose RGB and GBR selection order.

Sha et al. teaches RGB and GBR selection order (fig. 2B, item 51, col. 11, lines 43-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Sha et al. teachings into Nagai, Kim and Jeddeloh system in order to preprocess different formats (col.1, lines 16-21 in the Sha et al. reference).

Allowable Subject Matter

4. Claim 6-12,18-23,27-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claims 6,18,27 the major difference between the teaching of the prior art of record (Kim, Jeddeloh and Nagai) and the instant invention is that a subfield matrix for receiving the subfield data generated by the subfield data generator and output in series, converting the subfield data for a specific number of neighboring cells on the same line into parallel subfield data, and outputting the parallel subfield data to the frame memory.

Claims 19-23 depend on claim 18.

Relative to claims 7,28 the major difference between the teaching of the prior art of record (Kim, Jeddeloh and Nagai) and the instant invention is that the subfield data generator comprises a first subfield data generator and a second subfield data generator for respectively generating subfield data corresponding to two sets of video data selected from the RGB video data, and the subfield matrix comprises a first subfield matrix and a second subfield matrix for respectively receiving the subfield data output in series by the first and second subfield data generators, generating parallel subfield data corresponding to a specific number of neighboring cells, and outputting the parallel subfield data.

Claim 8 depends on claim 7.

Relative to claim 7 the major difference between the teaching of the prior art of record (Kim, Jeddeloh and Nagai) and the instant invention is that a data buffer for

Art Unit: 2629

receiving the subfield data generated by the subfield data generator, dividing the subfield data into two subfield data sets, providing the two subfield data sets to the frame memory using the rising edge and the falling edge of the reference clock signal, respectively, reading the subfield data sets using the rising edge and the falling edge, respectively, of the reference clock signal, and providing the two subfield data sets to the subfield data arranger.

Claims 10-12 depend on claim 9.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number: 10/840,169 Page 9

Art Unit: 2629

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS 04.18.07

> RICHARD HJERPE SUPERVISORY PATENT EXAMINER